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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,074	02/11/2004	Afshin Momtaz	51463/SDB/B600	2103

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

E/1

Office Action Summary	Application No.	Applicant(s)	
	10/776,074	MOMTAZ, AFSHIN	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3,7-9,17,18,22,23,30 and 31* is/are allowed.

6)☒ Claim(s) *1,2,4,10-12,15,19,20,24-28,32-35 and 37* is/are rejected.

7)☒ Claim(s) *5,6,13,14,16,21,29 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments with respect to claims 1-2, 4-5, 8, 10-12, 15-16, and 19-21 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 4, 10-11, 24-28, 32-35, and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Sari et al. (SARI, H., et al. 'Phase and Frequency Detectors for Clock Synchronization in High-speed Optical Transmission Systems. " European Transactions On Telecommunications and Related Technologies, vol. 5, no. 5, September - October 1994, pp. 101-107).

In reference to claim 1 Sari discloses in Figures 4-5 a binary phase detector comprising: a first flip flop (1) comprising: a data input coupled to a first signal (Received Signal/ Clock in Figure 4) having a first frequency, and a clock input coupled to a second signal (Recovered Clock (Input Signal in Figure 4)) having a second frequency, wherein the first frequency is a multiple of the second frequency; and a second flip flop (2) comprising: a data input coupled to the output of the first flip flop (1), and a clock input coupled to the second signal (Recovered clock). The same applies to claims 10-11, 25, 33, and 37.

In reference to claim 2, Sari discloses in Figure 5 wherein the first flip flop (1) is a high-speed flip-flop.

In reference to claim 4, Sari discloses in Figure 5 wherein the second flip flop (2) is a low speed flip flop.

In reference to claim 24, Sari discloses in Figures 4-5 that by the data input receiving the higher speed clock signal, each data input will provide a lower capacitive load than each clock input so that a lower capacitive load is provided to higher frequency signals than is provided to lower frequency signals. The same applies to claims 28, 32, and 35.

In reference to claim 26, Sari discloses in Figure 5 wherein an output of the second flip flop provides a binary indication of whether the first signal leads or lags the second signal.

In reference to claim 27, Sari discloses in Figure 5 wherein a signal at the data input of the low speed flip flop (2) is of a lower frequency than the first frequency such that the low speed flip flop is adapted to operate at a lower speed than the high speed flip flop. The same applies to claim 34.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12, 15, and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (U.S. Patent No. 6,388,485) in view of Sari et al. (SARI, H., et al. 'Phase and Frequency Detectors for Clock Synchronization in High-speed Optical Transmission Systems. " European Transactions On Telecommunications and Related Technologies, vol. 5, no. 5, September - October 1994, pp. 101-107).

In reference to claim 15, Kim discloses in Figure 3 a delay lock loop comprising: phase detector; digital filter (342), coupled to receive the at least one phase error signal (DS through controller 324), that generates at least one filtered signal (DCON2); and a phase rotator (344), coupled to receive the at least one filtered signal (DCON2) and the second signal (ECLK), that delays the second signal according to the at least one filtered signal (DCON2). Kim does not disclose that the phase detector comprises a first and second flip-flop. Sari discloses a phase detector as mentioned above with respect to claim 1. It would have been obvious to one skilled in the art at the time of the invention that the binary phase detector of Sari could be used in the circuit of Kim as the phase detector for the advantage of being able to decrease design time by using a well known design for a phase detector. The same applies to claim 19, wherein Kim discloses in column 5, lines 49-50 (with reference to Figure 5) that the delay controller is implemented as a charge pump and the loop filter is seen to be element 542. The same also applies to claim 12, wherein all the limitations of the base claim and any intervening claims are met by Sari as mentioned above with reference to claim 10.

In reference to claim 20 the delay circuit (544 of Kim) comprises at least one delay line.

Allowable Subject Matter

6. Claims 3, 7-9, 17-18, 22-23, and 30-31 are allowed.

7. Claims 5-6, 13-14, 16, 21, 29, and 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Claims 5-6, 16, 21, 29, and 36 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 8 wherein the high speed flip flop comprises a high speed latch (710) and a low speed latch (720) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 13 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 8 wherein the first, second, and output signal comprise differential signals in combination with the rest of the limitations of the base claims and any intervening claims. Claims 14 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 8 wherein the circuit comprises an inductive load (L1, L2) for the first flip flop (710) in combination with the rest of the limitations of the base claims and any intervening claims.

9. The following is an examiner's statement of reasons for allowance: Claims 3, 9, 17, and 22 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 8 wherein the circuit comprises an inductive load (L1, L2) for the first flip flop (710) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 7, 18, and 23 are allowed because the closest prior art of

record fails to disclose a circuit as shown in Figure 8 wherein the first, second, and output signal comprise differential signals in combination with the rest of the limitations of the base claims and any intervening claims. Claims 8 and 30-31 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 8 wherein the high speed flip flop comprises a high speed latch (710) and a low speed latch (720) in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

February 4, 2006

TIMOTHY P. CALLAHAN
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